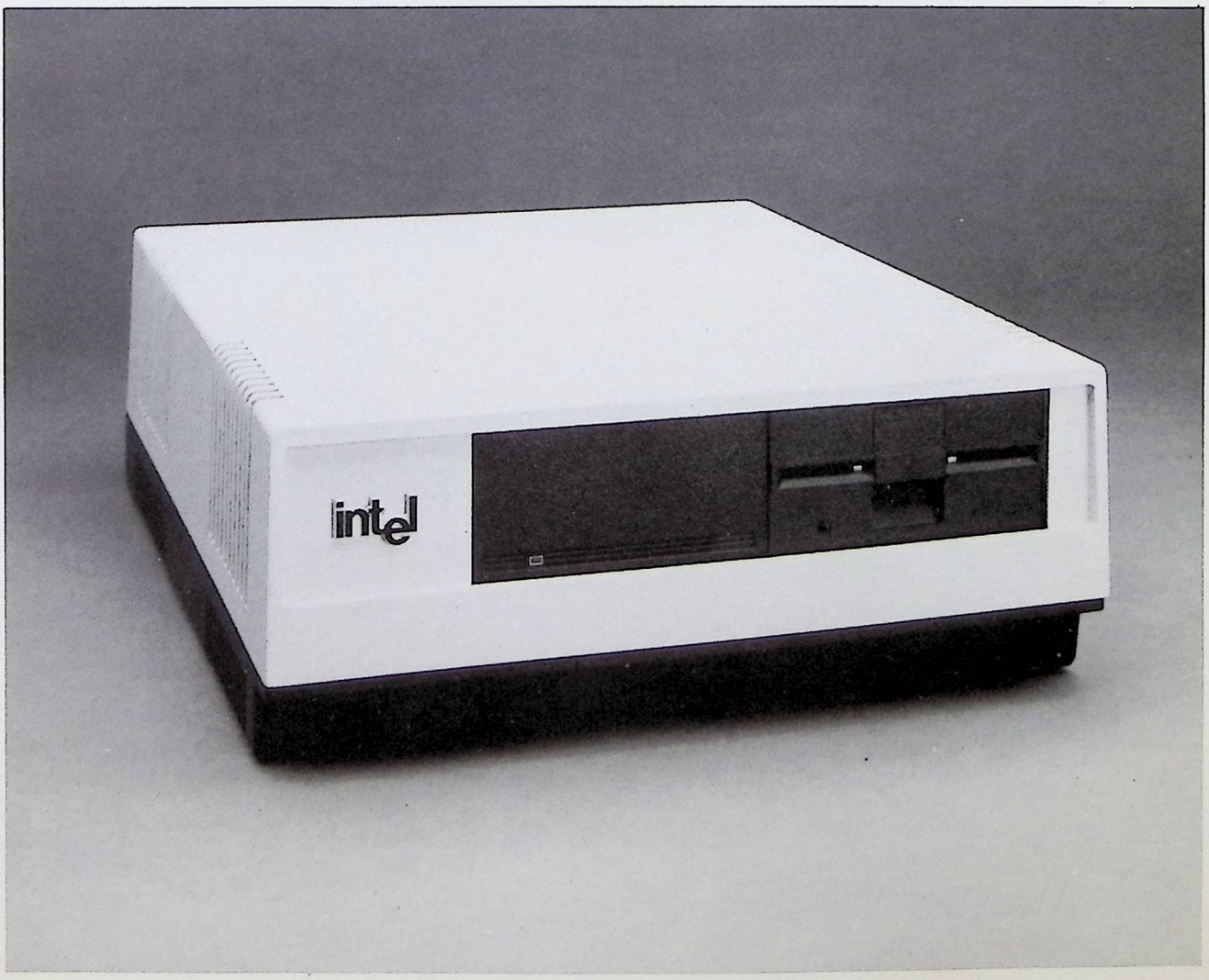
SYSTEM 310
MEMORY CONFIGURATION GUIDE: 86-BASED SYSTEMS



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 173206-001

SYSTEM 310
MEMORY CONFIGURATION GUIDE: 86-BASED SYSTEMS

Order Number: 173206-001

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

The information in this document is subject to change without notice.

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update or to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

Intel software products are copyrighted by and shall remain the property of Intel Corporation. Use, duplication or disclosure is subject to restrictions stated in Intel's software license, or as defined in ASPR 7-104.9 (a) (9).

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Intel Corporation.

Intel Corporation makes no warranty for the use of its products and assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

Intel retains the right to make changes to these specifications at any time, without notice.

Contact your local sales office to obtain the latest specifications before placing your order.

The following are trademarks of Intel Corporation and its affliates and may be used only to identify Intel products:

BITBUS	iLBX	iPDS	Plug-A-Bubble
COMMputer	i_m	iRMX	PROMPT
CREDIT	iMMX	iSBC	Promware
Data Pipeline	Insite	iSBX	QUEX
Genius	int_el	iSDM	QUEST
$\frac{\Delta}{1}$	Int_elBOS	iSXM	Ripplemode
	Intelevision	Library Manager	RMX/80
i	$int_eligent$ Identifier	Megachassis	RUPI
I^2ICE	$int_eligent$ Programming	MICROMAINFRAME	Seamless
ICE	Intellec	MULTIBUS	SOLO
iCS	Intellink	MULTICHANNEL	SYSTEM 2000
iDBP	iOSP	MULTIMODULE	UPI
iDIS			

MDS is an ordering code only and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corporation.

MULTIBUS is a patented Intel bus.

Printed in USA/IS-032/5.5k/1083/WCP
OEM Systems

REV.	REVISION HISTORY	DATE
-001	Original issue	10/83

CAUTION

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A Computing Device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

This manual discusses random access memory (RAM) in 86-based System 310's. First it outlines the system memory map and explains which board combinations have been verified by Intel. Next, it provides some background information about the three boards Intel recommends. Then, it provides jumper and installation instructions so you can add boards, remove boards, or change the address of memory in your system.

Specifically, this manual explains how to configure three memory boards: the iSBC® 012B Memory Board, the iSBC 056A Memory Board, and the iSBC 304 RAM Expansion MULTIMODULE™ Board.

THE CHAPTERS AT A GLANCE

Chapter 1 - Configuring Memory
Shows the suggested System 310 memory map and shows several valid RAM board combinations guided by the map. Identifies the RAM board combinations that are part of a preconfigured system.

Chapter 2 - Operating Features
Overviews the operating features of several System 310-compatible memory boards.

Chapter 3 - Setting the Jumpers on the 012B Board
Lists and explains required jumper settings on the 012B memory board.

Chapter 4 - Setting the Jumpers on the 056A Board
Lists and explains required jumper settings on the 056A memory board.

Chapter 5 - Removing and Installing Memory Boards
Lists step-by-step instructions for installing and removing the 012B and the 056A memory boards in the System 310 cardcage.

Appendix A - 012B Memory Board Revision Differences
Furnishes conversion drawings showing the differences between the jumper designations on the previous version of the 012B memory board and the updated one. Enables you to follow the installation instructions regardless of which version board you have.

Appendix B - 012B Board Operating Specifications
Provides electrical, mechanical, and environmental operating specifications.

Appendix C - 056A Board Operating Specifications
Provides electrical, mechanical, and environmental operating specifications.

RELATED PUBLICATIONS

The following manuals contain detailed information about the products discussed in this manual. You can order copies by contacting the Intel Literature Department at the address listed on page ii of this manual.

iSBC 012B Technical Manual, Order Number 112748

iSBC 016A/032A/064A/028A/056A RAM Board Hardware Reference Manual, Order Number 143572

iSBC 86/14 and iSBC 86/30 Single Board Computer Hardware Reference Manual (also covers the iSBC 304 MULTIMODULE board), Order Number 144044

System 310 Processor Configuration Guide: iSBC 86/30 Single Board Computer, Order Number 173205

System 310 Hardware Integration Guide, Order Number 173203

System 310 Publications Guide, Order Number 173441

United States customers may obtain service and repair assistance by contacting the Intel Product Service Center in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information.

Before calling the Product Service Center you should have the following information:

- The date you received the product.
- The complete part number (including the dash number) of the product. This number is usually silk-screened onto printed circuit boards and stamped on the label of other products.
- The serial number of the product. This is usually silk-screened onto printed circuit boards and stamped on the label of other products.
- Your shipping and billing addresses.
- A purchase order number for billing purposes if your Intel product warranty has expired.
- Extended warranty agreement information, if applicable.

SERVICE AND REPAIR ASSISTANCE

Use the following telephone numbers to contact the Intel Product Service Marketing Administration group:

	Regional Telephone Numbers	TWX Numbers
Western Region	(602) 869-4951	910-951-1330
Midwestern Region	(602) 869-4392	910-951-0687
Eastern Region	(602) 869-4045	
International	(602) 869-4391	

Always contact the Intel Product Service Marketing Administration group before returning a product to Intel for repair. When you make the request you will be given a repair authorization number, shipping instructions, and other information that will help Intel provide you with fast, efficient service.

If you are returning a product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate repair.

Use the original factory packaging material in preparing a product for shipment to the repair center. If that material is not available, ensure the product is adequately protected by wrapping it in cushioning material before enclosing it in a heavy-duty corrugated shipping carton. All cartons should be labeled "FRAGILE" to ensure careful handling. If a printed circuit board is being returned, a material such as Air Cap TH-240, manufactured by the Sealed Air Corporation of Hawthorne, New Jersey, should be used to give adequate cushioning.

Address and ship only to the address specified by Intel Product Service Marketing Administration group personnel.

CONTENTS

TABLES

FIGURES

CHAPTER 1
CONFIGURING MEMORY

This chapter is an overview of the memory in the 86-based System 310. It presents the 86-based System 310 memory map. It also lists the amount of memory in several preconfigured systems. This same list provides information about combining memory boards so you can expand memory but not violate the memory map requirements.

ADDRESSABLE MEMORY SPACE

Each System 310, whether you buy it preconfigured from Intel or you modify it yourself, contains random access memory (RAM) that you can use for your software. In 86-based systems, RAM can reside on the iSBC® 86/30 Single Board Computer (the processor board), the iSBC 304 RAM MULTIMODULE™ board, and on two MULTIBUS® boards: the iSBC 012B Memory board and the iSBC 056A Memory board.

Although the 8086 CPU addresses up to one megabyte of memory, not all of that space is available to you. The System 310 reserves space for RAM and for firmware which contains the iSDM™ 86 monitor, the bootstrap loader, and the System Confidence Test (SCT). Figure 1-1 shows these system requirements as a memory map.

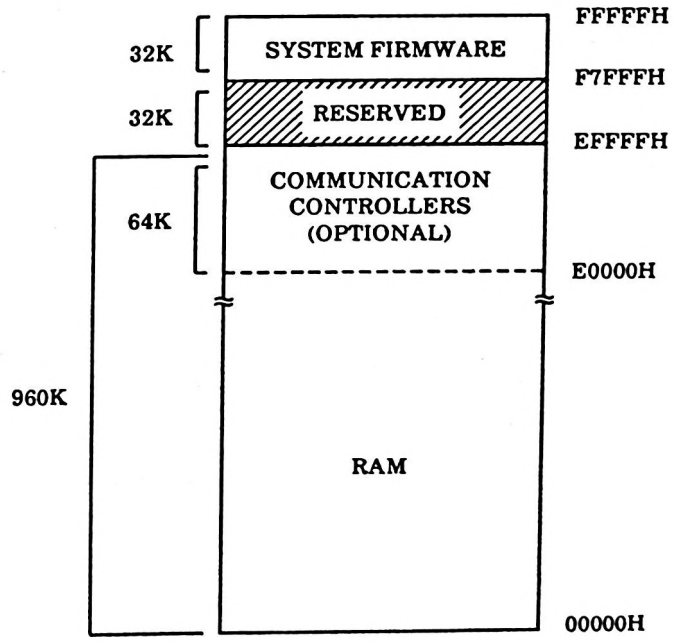


Figure 1-1. Memory Map in Hex F-0041

EXPANDING MEMORY

As mentioned previously, you can add memory boards to the System 310 to increase its memory size. When modifying your own system memory, you can add or remove boards, or combine them with the iSBC 056A memory board (a compatible board not supplied as part of a preconfigured system). Memory can be added up to a total of 1 megabyte, the upper limit of memory that the 8086 CPU can directly address.

GENERAL RULES FOR ALTERING MEMORY

Be sure to follow these general rules when changing the memory configuration of your system:

- The System 310 expects contiguous RAM. Although there must be a gap between the top of RAM and the memory you use for intelligent communications controllers (typically located at E0000H), make sure there are no gaps in the address space from 00000H to the top of RAM.
- The bootstrap loader needs RAM at 00000H.
- If using more than one full-sized MULTIBUS memory board, you must relocate the status/error register on one of the boards, or the parity error information it contains may be incorrect. This is done with jumpers and explained in Chapter 3.

Table 1-1 itemizes the System 310 memory boards and provides information you need to add or remove memory in your system. It lists the amount of memory each board provides and the board's address range. This manual refers to the combinations in this table in later chapters.

NOTE

Table 1-1 shows the memory boards arranged with their address ranges starting in a particular order. Chapters 3 and 4 explain how to jumper the memory boards for only these addresses.

While it is certainly possible to change the order of the memory boards from the one shown here, you may need to refer to the product manuals listed in the Preface for more jumper information.

Table 1-1 presents eight tested combinations of memory boards. Each combination provides the most memory at the least cost, measured in space consumed and dollars. For instance, the 304 MULTIMODULE board adds 128K bytes of memory to the system but does not consume a card slot because it fastens directly onto the processor board. On the other hand, both the 056A and 012B boards require one slot each, but they add a substantial amount of memory.

Table 1-1. Valid Memory Board Combinations

Total Size (System)	Board Name and Size in Bytes	Address Range in Hex
Combination 1 128K Bytes (310-1)	86/30 processor, 128K	00000-1FFFF
Combination 2 256K Bytes (310-2)	86/30 processor, 128K 304 MULTIMODULE, 128K	00000-1FFFF 20000-3FFFF
Combination 3 384K Bytes	86/30 processor, 128K 056A memory, 256K	00000-1FFFF 20000-5FFFF
Combination 4 512K Bytes	86/30 processor, 128K 304 MULTIMODULE, 128K 056A memory, 256K	00000-1FFFF 20000-3FFFF 40000-7FFFF
Combination 5 640K Bytes (310-3)	86/30 processor, 128K 012B memory, 512K	00000-1FFFF 20000-9FFFF
Combination 6 768K Bytes	86/30 processor, 128K 304 MULTIMODULE, 128K 012B memory, 512K	00000-1FFFF 20000-3FFFF 40000-BFFFF
Combination 7 896K Bytes	86/30 processor, 128K 056A memory, 256K 012B memory, 512K	00000-1FFFF 20000-5FFFF 60000-DFFFF
Combination 8 960K Bytes	86/30 processor, 128K 304 MULTIMODULE, 128K 056A memory, 256K 012B memory, 384K	00000-1FFFF 20000-3FFFF 40000-7FFFF 80000-EFFFF




CHAPTER 2
OPERATING FEATURES

This chapter briefly discusses the operating features of each of three System 310-compatible memory boards: the iSBC 012B memory board, the iSBC 056A memory board, and the iSBC 304 MULTIMODULE board.

Since the System 310 does not use every feature these boards can provide, this chapter compares the available features with the features actually used by the System 310. It further notes which features are controlled by jumpers in case you want to add a feature not currently implemented in the preconfigured systems. See Chapter 3 for specific jumper changes.

DYNAMIC RAM CAPACITY

The three memory boards recommended for the System 310 provide a range of memory from small to large. The smallest increment you can buy is the 304 MULTIMODULE board which supplies 128K bytes of RAM and fastens directly onto the processor board. In the middle-sized range, the 056A board supplies 256K bytes of RAM, and at the high end, the 012B board supplies 512K bytes of RAM. Both the 012B and the 056A boards are addressable on 4K boundaries.

All RAM must be addressed as a contiguous block and jumpers select the starting and ending addresses of the block. These address select jumpers are found on the 012B board and the 056A board. The address range for the 304 board is controlled with jumpers on the 86/30 processor board.

AUTOMATIC ON-BOARD REFRESH

The 012B and the 056A boards automatically refresh their RAM with an on-board pulse generator so that you do not have to provide these signals. The processor board provides the refresh signals for its RAM and the 304 MULTIMODULE board (when installed).

If you want to provide off-board refresh signals, however, you can change the memory refresh jumper settings on the memory boards. You cannot supply off-board refresh to the processor board. In addition, you will have to supply a dual auxiliary bus connector (also known as a P2 connector) to connect your refresh logic circuit to the bus.

PARITY ERROR DETECTION

While the System 310 memory does not interrupt the CPU on a parity error, the 012B and 056A boards detect and report errors in an 8-bit status/error register. Parity errors cause on-board LEDs to light up as a signal that an error has occurred, although you cannot see the LEDs unless you remove the back panel. At this signal, you can read the parity errors from this status/error register by issuing an I/O command in your software. Refer to the individual manuals for the memory board products listed in the Preface for the meaning of these lights.

The location of the status/error register depends on the kind of memory boards you use. When either one 012B board or one 056A board is installed in the System 310, the address of the status/error register is 00000H. However, two boards cannot use the same address for the status/error register. So, when combining two boards, such as an 012B board and an 056A board (combination 7 from Table 1-1), use jumpers to change the address of the status/error register on one of the boards.

The 304 board does not provide parity error detection, nor does the RAM on the processor board.

CHAPTER 3
SETTING THE JUMPERS ON THE 012B BOARD

This chapter explains the jumper settings for the iSBC 012B Memory Board. First, it provides a list of jumper-controlled parameters. This list is similar, but more detailed, than the feature list mentioned in the second chapter. Next, a drawing shows where jumpers are located. From there, categories shown in the drawing become the topic of separate sections explaining what each jumper does and when you might want to change its setting.

These individual sections refer back to the memory board combinations in Table 1-2. For example, in the section on address select jumpers, you will find out how to jumper the 012B board for the address ranges in combinations 5, 6, 7, and 8; these are all the combinations that use the 012B board.

NOTE

Jumper designations on the previous version of the 012B board are different from the jumper designations on the updated version. Previous versions have a W printed in front of each jumper number. The jumper function and the location of each connection are the same, only the labels have changed.

The examples and tables in this manual use the updated board numbers. However, Appendix A compares the previous and the updated numbers so you can convert.

JUMPER-SELECTABLE PARAMETERS

Figure 3-1 shows an outline of the 012B memory board, jumpered for the System 310-3. The categories shown in this figure, and listed below, represent the operating parameters that are controlled by jumper settings.

- Address select jumpers--select the starting and ending addresses of memory
- Segment select jumpers--select the specific 4-megabyte segment that memory occupies
- Full- or half-memory size select jumpers--select whether or not to use all or one-half of the memory chips on the board
- I/O address select jumpers--select the location of the status/error register

Other functions, such as battery backup and parity error interrupts, are not used by the System 310 and, therefore, are only briefly covered in this manual. You can find detailed information in the *iSBC 012B Technical Manual* listed in the Preface.

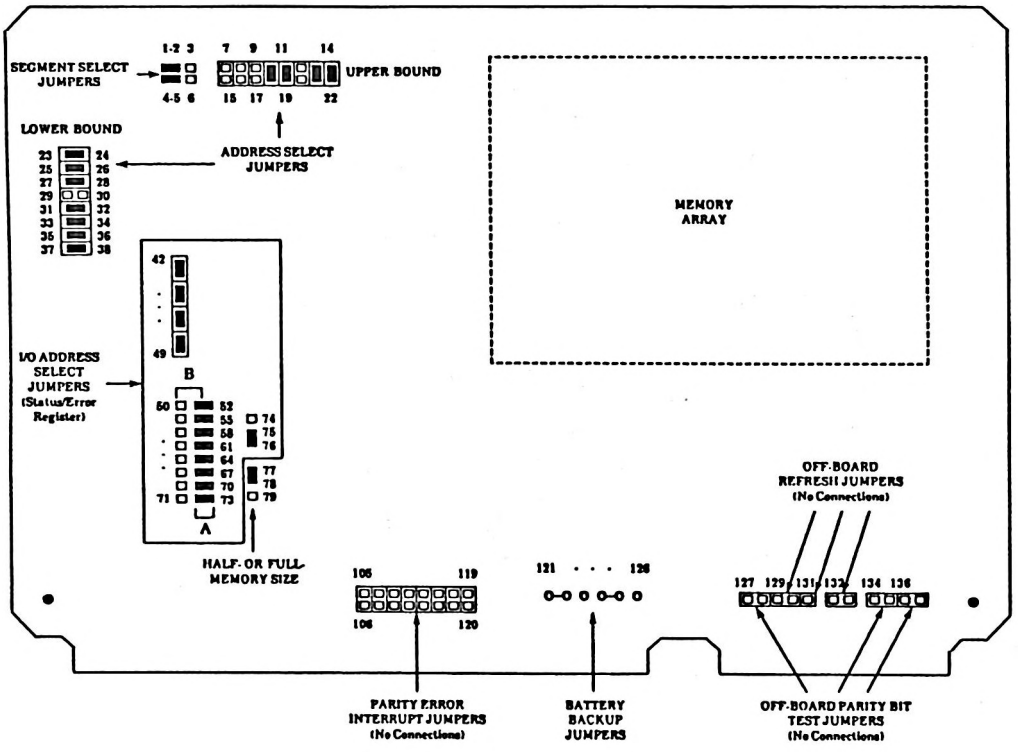


Figure 3-1. Jumper Locations on the 012B Board F-0007

ADDRESS SELECT JUMPERS

Two sets of jumpers select the address range for the 012B memory board. The first set, labeled "upper bound" and "lower bound" in Figure 3-1, selects the starting and ending addresses of the 512K-byte block of memory found on this board. Specifically, lower bound jumper settings determine the starting address, and upper bound settings determine the ending address. You will find these jumpers in the upper left corner of the board, labeled 7 through 38 (shown in Figure 3-1).

The second set of jumpers, labeled "segment select jumpers" in Figure 3-1, assigns memory locations to segments. These jumpers are covered later in the "Segment Select Jumpers" section.

The next four subsections describe the jumper settings for tested memory combinations that include an 012B board, combinations 5, 6, 7, and 8. Refer to Table 1-1 in Chapter 1 for a complete description of these memory combinations.

COMBINATION 5--THE 012B AND PROCESSOR BOARDS

The total number of bytes of RAM (640K) in combination 5, or System 310-3, is the sum of the memory on the 86/30 processor board and the memory on the 012B board. The processor board contributes 128K bytes, preset from address 00000H through 1FFFFH. The *System 310 Processor Configuration Guide: 86/30 Single Board Computer* contains specific jumper settings for these addresses. The 512K bytes of memory on the 012B board range from 20000H to 9FFFFH in this combination. Table 3-1 shows the jumper settings for this arrangement.

Table 3-1. 012B Jumpers for Address Range 20000H-9FFFFH

Upper Bound		Lower Bound	
Jumper	Connection	Jumper	Connection
7-15	-	23-24	X
8-16	-	25-26	X
9-17	-	27-28	X
10-18	X	29-30	-
11-19	X	31-32	X
12-20	-	33-34	X
13-21	X	35-36	X
14-22	X	37-38	X

Note: "X" means connected to ground. "-" means not connected.

COMBINATION 6--THE 012B, PROCESSOR, AND 304 BOARDS

Combination 6, although not part of a preconfigured system, contains 768K bytes of RAM. It consists of 128K bytes from the processor board plus 128K bytes from the 304 MULTIMODULE board, and 512K bytes from the 012B board.

The advantage of combining boards this way is that you can add memory without consuming an extra card slot. Simply mounting the 304 board directly onto the processor board. The jumpers on the processor board determine the starting and ending addresses for this combined 256K-byte block.

To complete the arrangement for combination 6 and maintain the required continguous block of RAM, address the processor board/MULTIMODULE board assembly from 00000H through 3FFFFH. (See the *System 310 Processor Configuration Guide: 86/30 Single Board Computer* for the jumper changes.) Then, address the 012B board starting at the next available location, 40000H through BFFFFH. Table 3-2 shows how to set the jumpers on the 012B board for these addresses.

Table 3-2. 012B Jumpers for Address Range 40000H-BFFFFH

Upper Bound		Lower Bound	
Jumper	Connection	Jumper	Connection
7-15	-	23-24	X
8-16	-	25-26	X
9-17	-	27-28	X
10-18	-	29-30	X
11-19	X	31-32	-
12-20	-	33-34	X
13-21	X	35-36	X
14-22	X	37-38	X

Note: "X" means connected to ground. "-" means not connected.

COMBINATION 7--THE 012B, PROCESSOR, AND 056A BOARDS

You can expand memory to 896K bytes by using the three boards listed as combination 7 (from Table 1-1). Address the boards so that the the processor board memory block is lowest, followed by the 056A, then the 012B boards.

Address the 128K bytes of memory on the processor board from 00000H through 1FFFFH, as recommended for all tested configurations. Following this convention, you will not have to change address jumpers on the processor board unless you are adding or removing a 304 board.

Since it is not efficient to use the 304 board as part of this combination, use the 056A and the 012B boards instead. Address the 256K bytes of RAM on the 056A board from 20000H to 5FFFFH. Table 1-1 shows that the 056A board usually occupies this space in the System 310. See Chapter 4 for jumpering instructions for the 056A board.

To jumper the 012B board so it occupies the top of the 896K-byte block of contiguous memory (60000H through DFFFFH), remove or connect the jumpers listed in Table 3-3.

Table 3-3. 012B Jumpers for Address Range 60000H-DFFFFH

Upper Bound		Lower Bound	
Jumper	Connection	Jumper	Connection
7-15	-	23-24	X W25
8-16	-	25-26	X W26
9-17	-	27-28	X W27
10-18	X W20	29-30	-
11-19	-	31-32	-
12-20	-	33-34	X W30
13-21	X W23	35-36	X W31
14-22	X W24	37-38	X W32

Note: "X" means connected to ground. "-" means not connected.

COMBINATION 8--THE 012B, PROCESSOR, 304, AND 056A BOARDS

To fully expand memory to 960K bytes, you must use all the boards mentioned in this manual. Locate the processor board's memory at the lowest address, followed by the memory on the 304 board. Then, fill the next highest space, from 40000H through 7FFFFH, with the 056A board. Top off the block with the 012B board, ranging from 80000H through EFFFFH.

To address these boards, refer to Chapter 4 for the jumper changes to the 056A board. Table 3-4 shows how to jumper the 012B board for these combination-8 addresses.

As an aside, notice that the total number of bytes available using this combination of boards is 1024K. However, the 86-based System 310's only allow 960K bytes of RAM total. Therefore, this board arrangement does not use all of the available RAM on the 012B memory board.

Table 3-4. 012B Jumpers for Address Range 80000H-EFFFFH

Upper Bound		Lower Bound	
Jumper	Connection	Jumper	Connection
7-15	-	23-24	X
8-16	-	25-26	X
9-17	X	27-28	X
10-18	-	29-30	X
11-19	-	31-32	X
12-20	-	33-34	-
13-21	X	35-36	X
14-22	X	37-38	X

Note: "X" means connected to ground. "-" means not connected.

SEGMENT SELECT JUMPERS

Segment select jumpers assign the RAM on the 012B board to one of four pages; each page is 4 megabytes long. Once assigned, the RAM block addresses begin on that specific page boundary. Since the 86-based System 310's address only 1 megabyte of memory, these jumpers are always preset to select the page with the lowest starting address, segment 1.

Table 3-5 shows the jumper connections that select each segment on the 012B board; two pairs are needed. If you use this board in a system capable of addressing more than 4 megabytes, such as the 286-based System 310, select any of the page boundaries shown in this table.

Table 3-5. 012B Board Segment Select Jumpers

Jumpers Connected	Segment Selected	Address Range in Hex
1-2, 4-5 (W33A-W33B, W34A-W34B)	1	000000-3FFFFF
2-3, 4-5	2	400000-7FFFFF
1-2, 5-6	3	800000-BFFFFF
2-3, 5-6	4	C00000-FFFFFF

HALF- OR FULL-MEMORY SIZE

You can use all four 64K banks of memory on the 012B board or mask off half (two banks) with the half- or full-memory size jumpers. These three jumpers are named for a signal line found on the 012B board schematics.

Preconfigured 012B boards have all 512K bytes available, so they have jumpers 77 and 78 connected. Replacing that connection with one between 78 and 79 disables the bottom two rows of memory chips (the rows closest to the card edge connector), leaving half of the memory available.

I/O ADDRESS SELECT JUMPERS

The jumpers in the I/O address select area, shown in Figure 3-1 and listed in Table 3-6, determine the address of the 8-bit status/error register. The status/error register logs parity error information that you can read with an I/O command in software. The 012B boards have this address preset to 00000H. If you add another 012B board, or an 056A board that also has this register set at 00000H, you must relocate one of the boards or the information in the register may not be valid.

Table 3-6 lists the jumper connections found in preconfigured System 310's. It also lists the significant address lines for the status/error register that are not determined by jumpers. The first column lists the address of the status register, from least to most significant bit, when the corresponding jumper pair in the second column is connected. The third column lists the names of the signal lines.

Table 3-6. 012B Board I/O Address Select Jumpers

Status/Error Register Address	Connection		Signal Name
0 (low)	42-43	W1	AD00
0 (low)	44-45	W2	AD01
0 (low)	46-47	W3	AD02
0 (low)	48-49	W4	AD03
0 (always low)	No jumper		AD04
0 (always low)	No jumper		AD05
0 (low)	75-76	W6	AD06*
0 (always low)	No jumper		AD07
0 (low)	51-52	W14A	AD08
0 (low)	54-55	W13A	AD09
0 (low)	57-58	W12A	AD0A
0 (low)	60-61	W11A	AD0B
0 (low)	63-64	W10A	AD0C
0 (low)	66-67	W9A	AD0D
0 (low)	69-70	W8A	AD0E
0 (low)	72-73	W7A	AD0F

* AD06 can be changed to high by changing the connection shown to 74-75.

The four pairs of jumpers labeled 42 through 49 and one of the two pairs of jumpers labeled 74 through 76 (five jumpers in all) affect the first 8 bits of address—the low byte of a 16-bit address. For the set labeled 42 through 49, each installed jumper connects its address line to ground. When all five jumpers are connected, as they are in preconfigured boards, they select all zeros (00000H) for the address of the register. Therefore, to relocate the status/error register, simply remove one of the jumpers. For example, removing 42-43 means that line AD00 must now be high, so the new address of the register is 00001H.

The jumpers labeled 50 through 73 affect the upper byte of a 16-bit I/O address. Figure 3-1 shows these jumpers divided into two columns, A and B. Connecting all the pairs in column A, as they are in preconfigured systems, means that all 16 bits are significant in selecting the address of the status/error register. In fact, the high byte must be all zeros. Connecting the pairs in column B means the upper 8 bits are irrelevant. The bottom half of Table 3-6 lists the jumper connections for column A.

BATTERY BACKUP JUMPERS

Since the System 310 does not back up data with batteries, the jumpers that would connect a battery to the back-up circuit on the 012B memory board are not connected. Instead, preconfigured systems connect 124 to 125 and 121 to 122 for power.

PARITY ERROR INTERRUPT JUMPERS

The System 310 does not provide the software needed to permit parity errors to interrupt the processor. Therefore, the parity error interrupt jumpers, shown in Figure 3-1, are not connected. Refer to the *System 310 Processor Configuration Guide: 86/30 Single Board Computer* and the *iSBC 012B Technical Manual* for more information about jumpers and available interrupts.

CHAPTER 4
SETTING THE JUMPERS ON THE 056A BOARD

Like the 012B memory board, you can use the 056A memory board to expand the System 310 RAM space. This chapter describes the jumpers that are preset by the factory and the jumpers you must change to use this board.

The layout of the information in this chapter is similar to Chapter 3. First, this chapter provides a list of jumper-controller parameters. Then, it provides a master drawing of the board showing the location of the jumpers in the drawing grouped into related categories. The labeled categories become the topic for the next few sections, each section repeating the significant portion of the master drawing to show you which jumpers to change and where to find them.

JUMPER-SELECTABLE PARAMETERS

By adding or removing jumpers, you can control the parameters listed below. Since the System 310 does not usually contain an 056A memory board, you must configure this board yourself. Do not remove any default jumpers unless you are directed to do so in this manual or you have consulted the *iSBC 016A/032A/064A/028A/056A RAM Board Hardware Reference Manual* and understand the effect of the change.

Figure 4-1 shows four jumper areas found on the 056A memory board. No jumper connections are shown. The names of the jumper areas found in this figure are listed below, followed by a brief description. Later sections of this chapter explain each area and the effect of optional settings.

- Start Address Select Jumpers--select the starting address of memory
- Megabyte Page Select Jumpers--assign memory to one of 16 possible pages of memory, each 1 megabyte long
- Status/Error Register Jumpers--select the address of the status/error register
- Interrupt Jumpers--permit a parity error to interrupt the CPU

Only two of these jumper areas, the address select and the status/error register jumpers, control parameters you are likely to change when using this board in an 86-based System 310. They are discussed at length in this chapter. The other two areas shown in Figure 4-1, the interrupt jumpers and the megabyte page select jumpers, are only briefly covered in this manual. See the *iSBC 016A/032A/064A/028A/056A RAM Board Hardware Reference Manual* listed in the Preface for more information.

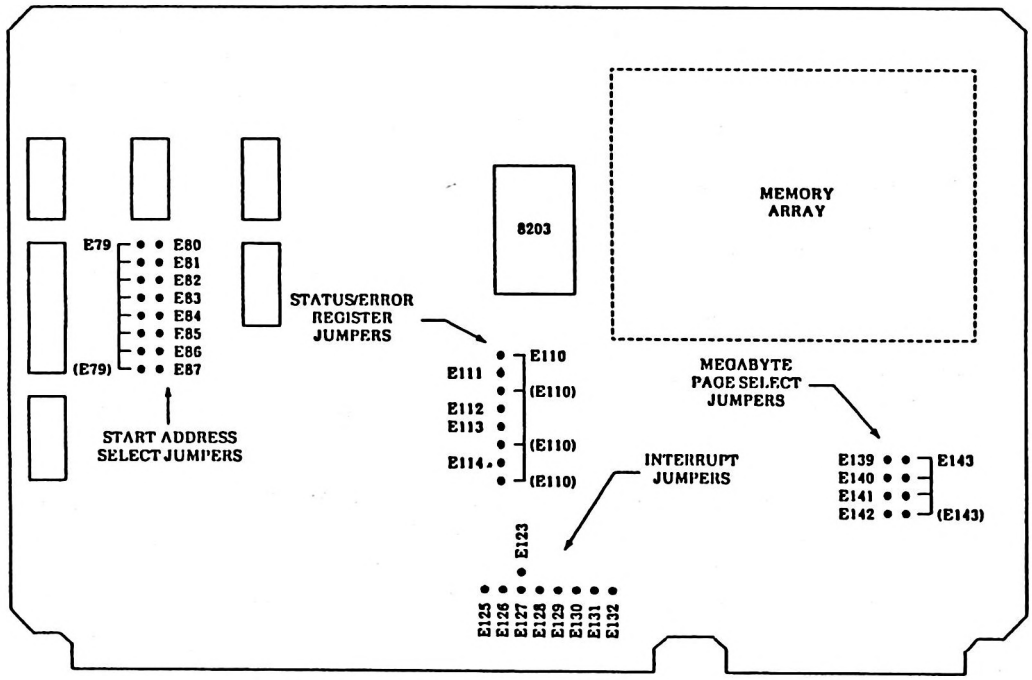


Figure 4-1. Jumper Locations on the 056A Board F-0011

START ADDRESS SELECT JUMPERS

The preconfigured 056A board does not select a starting address for you, so you must add jumpers in this area. The start address jumpers, with the megabyte page select jumpers, determine the beginning of the 256K bytes of memory on this board.

According to Table 1-1 in Chapter 1, the memory on the 056A memory board has two recommended address ranges. The first (combination 3) is from 20000H through 5FFFFH, just above the processor board's memory space. The second location (combination 4) is from 40000H through 7FFFFH, just above the combined processor board and 304 MULTIMODULE board memory space.

To configure the 056A board for these addresses, place the jumpers in the locations shown in either Figure 4-2 or 4-3. Figure 4-2 shows the jumpers that select starting address 20000H, and Figure 4-3 shows the jumpers that select starting address 40000H. The bracket in these drawings indicates that all the stake pins on the left side of the jumper block are electrically connected. In effect, they are all pin number E79. Therefore, when you connect a start address jumper, use the E79 pin closest to the stake pin representing the address you want.

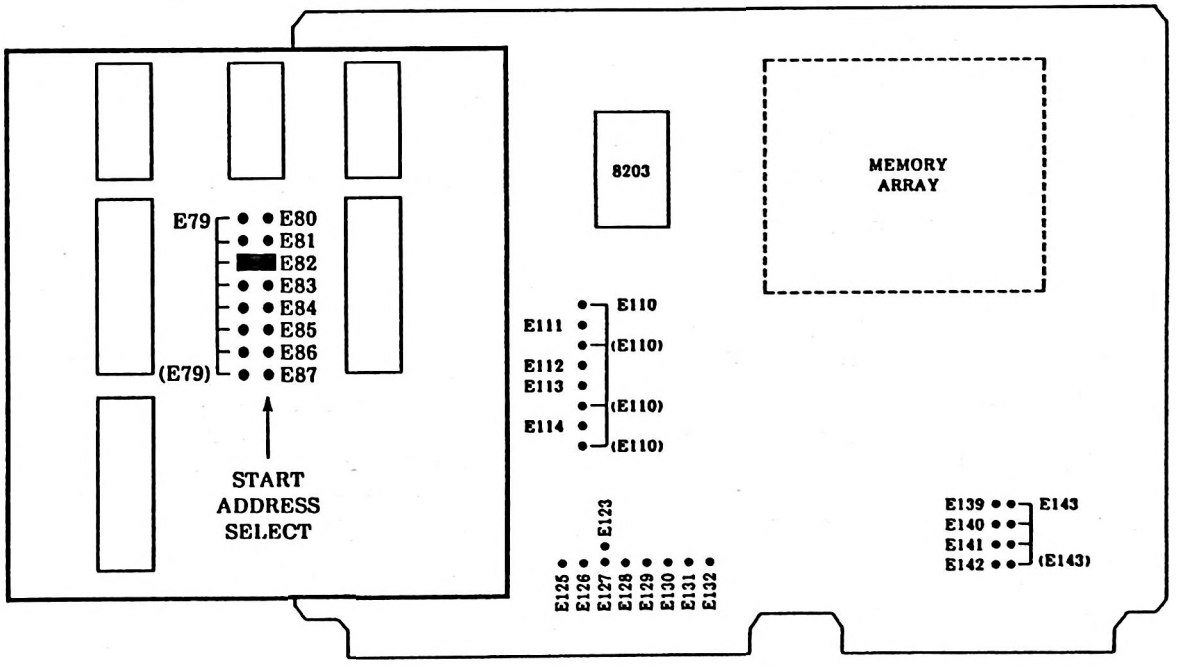


Figure 4-2. 056A Jumpers for Starting Address 20000H F-0098

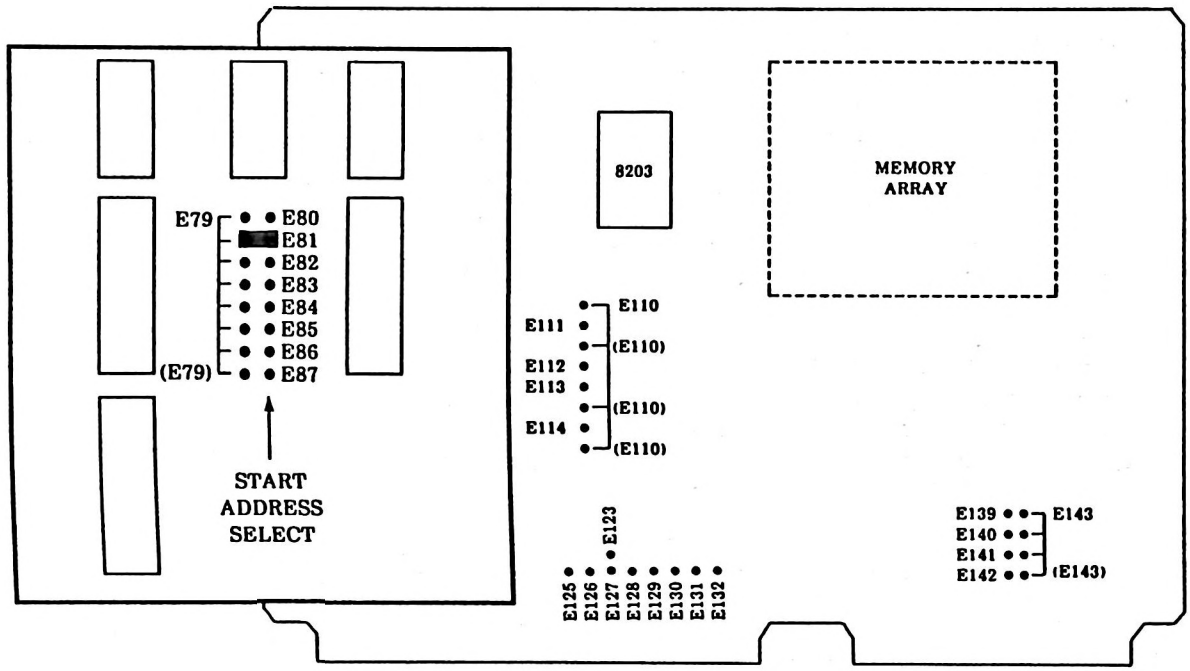


Figure 4-3. 056A Jumpers for Starting Address 40000H F-0099

MEGABYTE PAGE SELECT JUMPERS

The megabyte page select assigns the block of memory on this board into 1 of 16 possible pages; each page is 1 megabyte long. The factory does not place jumpers on any of the pins in this area. The absence of jumpers means that the system finds the RAM on this board in the lowest one-megabyte page. Since the 86-based System 310's address 1 megabyte at most, this configuration is recommended.

STATUS/ERROR REGISTER JUMPERS

Like the 012B board, the 056A board detects and reports parity errors. When it detects a parity error, it lights an LED and writes the location of the error in four bits of the byte-addressable status/error register.

In order to read this register with a software I/O command, you must first give it an address. Usually, the status/error register resides at 00000H. To select this starting address, connect four pairs of jumpers: E110 to E111, E110 to E112, E110 to E113, and E110 to E114. Figure 4-4 shows the location of these jumpers. Like the address select jumpers discussed in an earlier section, the bracket in this figure indicates that jumper E110 is made up of four stake pins, all electrically connected.

When you have two or more MULTIBUS RAM boards, such as a second 056A board or the 012B board, you must relocate the status/error register on one of them. This manual recommends that you relocate the 012B board, and it provides instructions for changing the jumpers (in Chapter 3). Refer to the *iSBC 016A/032A/064A/028A/056A RAM Board Hardware Reference Manual* for the jumper changes on this board.

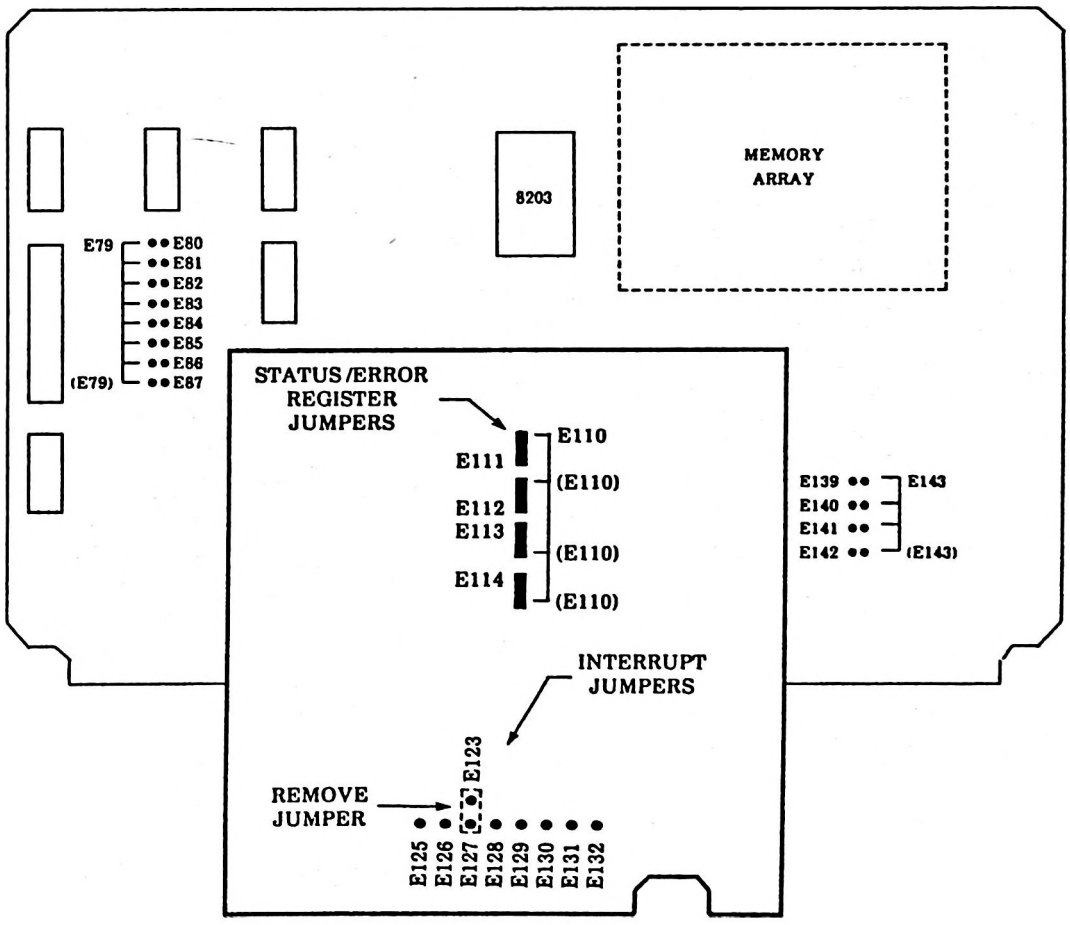


Figure 4-4. 056A Board Status/Error Register Jumpers F-0100

INTERRUPT JUMPERS

The interrupt request jumpers, when connected, permit a parity error detected by the 056A board to interrupt the CPU. Since no software drivers are provided for this feature in the System 310, you must either write this software yourself or remove the default jumper connecting E123 and E127. Figure 4-4 shows where this jumper is located.

CHAPTER 5
REMOVING AND INSTALLING MEMORY BOARDS

The steps in this chapter describe how to remove and install memory boards in the System 310 chassis. Of the three memory boards discussed in this manual, instructions are given for only two boards: the iSBC 012B memory board and the iSBC 056A memory board. The iSBC 304 RAM Expansion MULTIMODULE Memory Board is part of the iSBC 86/30 Single Board Computer hardware and its installation is covered in the *System 310 Processor Configuration Guide: 86/30 Single Board Computer*.

Follow the steps in this chapter when you need to:

- Rearrange the boards in the system
- Add boards to or remove boards from the system
- Service a memory board
- Change the jumper settings

Removing or installing boards takes about 20 to 30 minutes to complete.

WARNING

Unless you are a qualified service technician, do not attempt to service any parts in this system because of the risk of electrical shock. You can safely handle only those boards and jumpers that can be reached by removing the back panel of the chassis.

EQUIPMENT YOU WILL NEED

Phillips screwdriver for #6 and #8 Phillips screws.

REMOVING THE MEMORY BOARD

The next three sections describe the major steps for removing the memory boards from the System 310 chassis. Quite simply, you must open the chassis, disconnect the cables, and remove the board.

WARNING

To guard against a risk of fire, always disconnect the power cord before removing the chassis back panel.

OPENING THE CHASSIS

1. Turn off the power, then remove the AC power cord from the back of the System 310 chassis.

2. Turn the chassis so that the back panel is facing you.

3. Remove the four Phillips screws holding the back panel to the chassis. Save these screws and remember where they came from so you can reinsert them later.

4. Tilt the top of the back panel toward you and lift it out of the track at the bottom of the chassis. Be careful not to pull the back panel toward you so far that you disconnect the cables prematurely.

DISCONNECTING THE CABLES

Figure 5-1 shows the chassis with the back panel ajar and identifies the cables plugged into the processor board. The smaller one on the left is the serial port cable, and the larger one on the right is the parallel port cable. To remove any memory board, you must disconnect these cables as described in the next three steps.

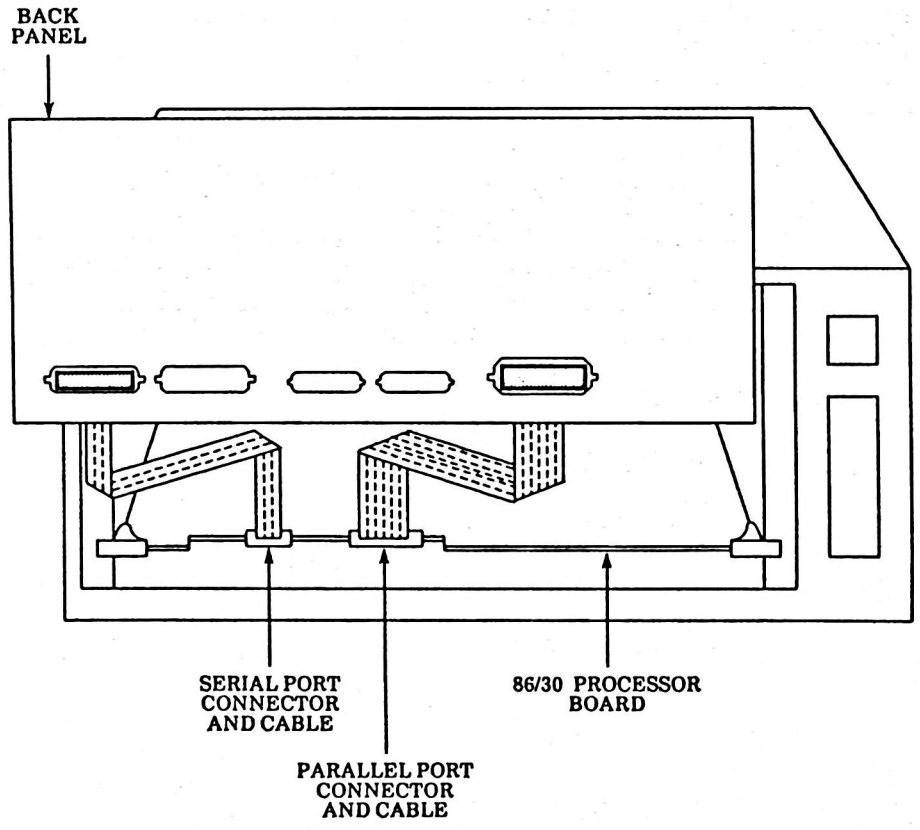


Figure 5-1. Installing the Serial and Parallel Port Cables F-0010

1. With one hand, raise the back panel until you can reach under it and into the cardcage. In the bottom card slot, you will see the 86/30 processor board with two cables plugged into it.

2. With your other hand, reach into the cardcage and disconnect these two cables. This frees the bottom of the back panel from the processor board. All other cables remain connected.

3. Flip the back panel over and lay it, connector side down, on top of the chassis. This keeps the back panel and any cables attached to it out of the way while you work inside the cardcage. Alternatively, you can remove all the cables and set the back panel aside. Be sure to mark or remember where the disconnected cables go so you can replace them.

WITHDRAWING THE BOARD FROM THE CARDCAGE

The next three steps describe how to remove a board from the edge connector at the back of the cardcage.

1. Loosen the screws that hold the two card retainers, shown in Figure 5-2. Lift each retainer up until it is free of the mounting screw and remove it. Save the retainers. These retainers prevent the cards from vibrating loose from the backplane during operation and transportation.

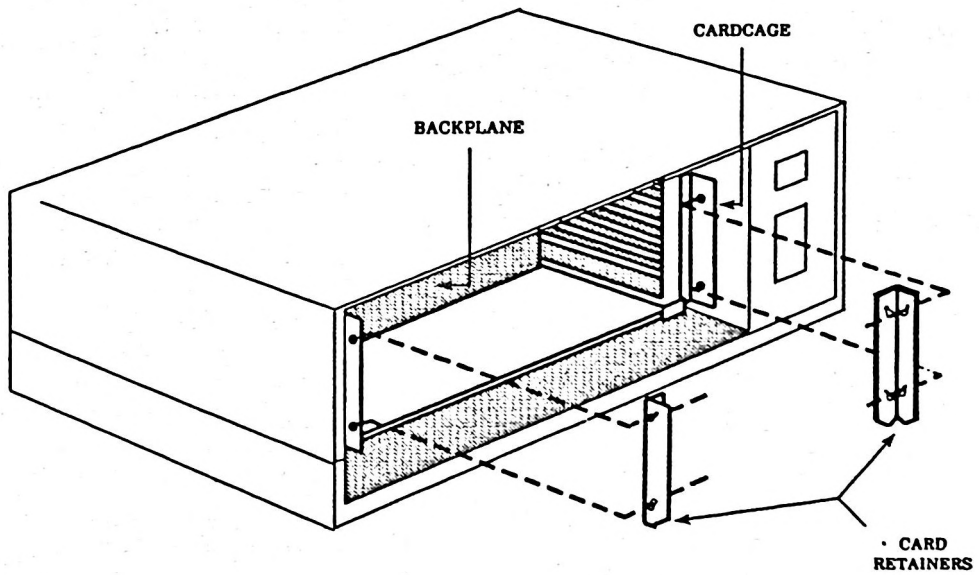


Figure 5-2. Removing the Card Retainers F-0087

2. Find the memory board in one of the slots shown in Table 5-1. This table lists board combinations described in Table 1-1, the name of the board, and the cardcage slot number Intel recommends you use for that board.

NOTE

Slots are numbered in order from the bottom of the cardcage to top. The bottom slot is slot 1.

3. Use the two card ejectors as levers to disconnect the board from the backplane. When the board "pops" out, pull the board free.

Table 5-1. Recommended Board Placement

Combination*	Board Type	Slot Number
3	86/30 Processor	1
	056A Memory	2
4	86/30 Processor	1
	304 MULTIMODULE	1
	056A Memory	2
5	86/30 Processor	1
	012B Memory	2
6	86/30 Processor	1
	304 MULTIMODULE	1
	012B Memory	2
7	86/30 Processor	1
	056A Memory	2
	012B Memory	3
8	86/30 Processor	1
	304 MULTIMODULE	1
	056A Memory	2
	012B Memory	3

* Refer to Table 1-1 in Chapter 1 for more information about memory board combinations.

INSTALLING MEMORY BOARDS

The four steps in this section explain how to install memory boards in the System 310 chassis.

1. Remove the back panel by following the steps listed earlier in this chapter in the section called "Opening the Chassis."

2. Once you have exposed the cardcage, insert the memory board in an available slot. (Refer to Table 5-1 for recommended board placement.) Be sure that the card edge connector of the memory board slides in first and that the component side is up. Push the memory board into the cardcage until it touches the backplane's edge connector.

3. To seat the board firmly in the edge connector, place your thumbs on the flat part of the card ejectors, pushing firmly until the card stops.

NOTE

Because of the weight of the 012B board, you may find it helpful to support it from the bottom, compensating for any sag, when inserting it in the card guide.

4. Test the connection by gently trying to pull the board out again. If you feel resistance, the board is securely seated. In addition, when the board is properly seated, the card ejectors rest flat against the cardcage. If the board slides forward, or the card ejectors are not flush against the cardcage, repeat step 3 above until these tests are met.

CLOSING THE CHASSIS

The seven steps in this section describe how to replace the back panel on the chassis. Essentially, it is the reverse of the removal process presented earlier in this chapter.

1. Install the card retainers and tighten the screws.

2. Connect the serial and parallel cables to the processor board. Although these ribbon cables are both marked P1, you can readily tell them apart by the number of conductors they contain. The parallel cable has 34 conductors, and the serial cable has 25 conductors.

   Plug the P1 connector of the parallel cable into the J1 port of the processor board; likewise, plug the P1 connector of the serial cable into J2 on the processor board. To correctly align the cables, be sure the P1 marks are upright. J1 and J2 are silkscreened onto the processor board. Figure 5-1 shows this placement.

3. Connect any other loose cables. Refer to the individual System 310 manuals listed in the Preface for details on cable routing.

4. Insert the bottom of the back panel into the track at the bottom of the chassis.

5. Carefully push the excess cable into the space between the boards and the back panel until the back panel fits flat against the chassis.

6. Align the screw holes in the back panel with the screw holes in the chassis, being sure not to pinch any cables, and replace the four screws you removed earlier. Since these screws are different sizes, be sure to replace the screws in the correctly sized holes.

7. Install the AC plug and turn the system on to run the system confidence tests (SCTs).

APPENDIX A
012B MEMORY BOARD REVISION DIFFERENCES

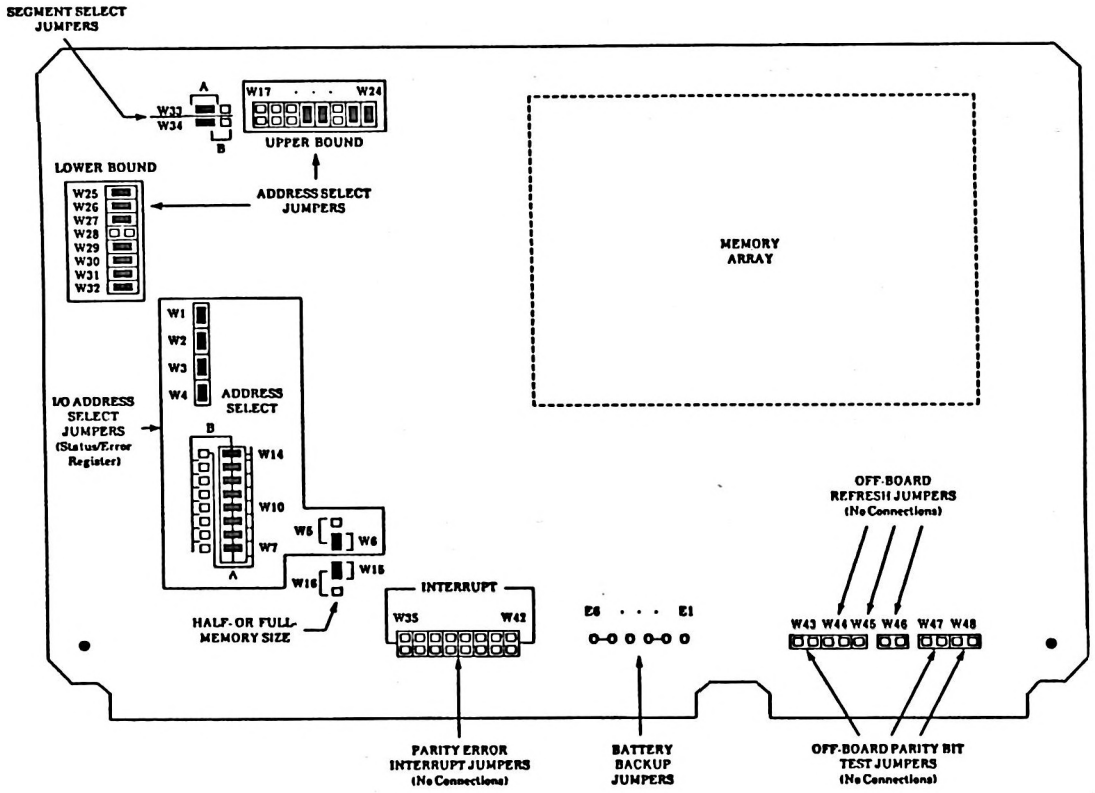
This appendix contains a table and a drawing of the jumper numbers on previous and current versions of the iSBC 012B memory board. You can tell if you have a previous version of the board because it will have a W written in front of most jumper numbers.

Table A-1 presents the connected jumper pairs that are shown in Figure 3-1 and Figure A-1, listed side-by-side so you can readily compare the previous numbers to the current numbers.

Table A-1. Previous and Current 012B Board Jumper Numbers

Current Jumper Numbers	Previous Jumper Numbers
1-2	W33A-W33B
4-5	W34A-W34B
10-18	W20
11-19	W21
13-21	W23
14-22	W24
23-24	W25
25-26	W26
27-28	W27
31-32	W29
33-34	W30
35-36	W31
37-38	W32
42-43	W1
44-45	W2
46-47	W3
48-49	W4
51-52	W14A
54-55	W13A
57-58	W12A
60-61	W11A
63-64	W10A
66-67	W9A
69-70	W8A
72-73	W7A
75-76	W6
77-78	W15
121-122	E6-E5
124-125	E3-E2

In the System 310, these two boards are functionally equivalent. The jumper connections and positions remain the same; only the jumper numbers have changed. If you have a previous version of this board, you can compare the jumper settings listed in Chapter 3 of this manual with the drawing and table in this appendix to see what the former number for that position was.



P-0007-1

Figure A-1. Former 012B Memory Board Jumper Numbers

STORAGE	512K bytes
BYTE SIZE	8 bits
WORD LENGTH	2 bytes
ACCESS TIME	350 ns
MEMORY CYCLE TIME	550 ns
REFRESH CYCLE TIME	550 ns
OPERATING MODES	Read Write Refresh (transparent to the user)
INTERFACE	TTL-compatible digital signals MULTIBUS interface
POWER FAIL PROTECTION	Circuitry for battery backup
POWER SUPPLY	
Voltage	+5.0 VDC ±5%
Operating Current	5.0 amps (maximum)
Standby Current	3.5 amps (maximum)
Power-Down Current	1.2 amps (maximum)
DIMENSIONS	
Length	6.75 inches
Width	12.0 inches
Height	0.50 inches
ENVIRONMENT	
Operating Temperature	0 to 55 °C
Relative Humidity	10 to 90% without condensation
Shock/Vibration	Able to withstand class B tests per Intel environmental specification 9400008 Rev. C
Altitude	Up to 15,000 feet in operation
POWER REQUIREMENTS	
Continuous Memory Cycles	25 watts (maximum)
Standby/Refresh Cycles Only	17.5 watts (maximum)
Battery Backup	6.0 watts (maximum)

APPENDIX C
056A BOARD OPERATING SPECIFICATIONS

STORAGE	256K bytes
BYTE SIZE	8 bits
WORD LENGTH	2 bytes
ACCESS TIME	
Read	570 ns
Write	363 ns
MEMORY CYCLE TIME	
Read	653 ns
Write	653 ns
Refresh	653 ns
INTERFACE	TTL-compatible digital signals MULTIBUS interface
POWER SUPPLY	
Voltage	+5.0 VDC
Operating Current	4.0 amps (maximum) 2.0 amps (typical)
POWER CONSUMPTION	24 watts (maximum) 10 watts (typical)
DIMENSIONS	
Length	6.75 inches
Width	12.0 inches
Height	0.50 inches
Weight	14.0 ounces
ENVIRONMENT	
Operating Temperatures	0 to 55° C
Operating Humidity	To 90% (without condensation)

intel®

REQUEST FOR READER'S COMMENTS

Intel's Technical Publications Departments attempt to provide publications that meet the needs of all Intel product users. This form lets you participate directly in the publication process. Your comments will help us correct and improve our publications. Please take a few minutes to respond.

Please restrict your comments to the usability, accuracy, organization, and completeness of this publication. If you have any comments on the product that this publication describes, please contact your Intel representative. If you wish to order publications, contact the Literature Department (see page ii of this manual).

1. Please describe any errors you found in this publication (include page number).

2. Does this publication cover the information you expected or required? Please make suggestions for improvement.

3. Is this the right type of publication for your needs? Is it at the right level? What other types of publications are needed?

4. Did you have any difficulty understanding descriptions or wording? Where?

5. Please rate this publication on a scale of 1 to 5 (5 being the best rating). _____

NAME _____ DATE _____

TITLE _____

COMPANY NAME/DEPARTMENT _____

ADDRESS _____

CITY _____ STATE _____ ZIP CODE _____

(COUNTRY)

Please check here if you require a written reply. ☐

WE'D LIKE YOUR COMMENTS . . .

This document is one of a series describing Intel products. Your comments on the back of this form will help us produce better manuals. Each reply will be carefully reviewed by the responsible person. All comments and suggestions become the property of Intel Corporation.

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 79 BEAVERTON, OR

POSTAGE WILL BE PAID BY ADDRESSEE

Intel Corporation
5200 N.E. Elam Young Pkwy.
Hillsboro, Oregon 97123

ISO-N Technical Publications

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 (408) **987-8080**

Printed in U.S.A.